

## CompSci 310 Computer Architecture Fall'08

**Instructor:** George Georgiev

**Office:** HS, Room 217

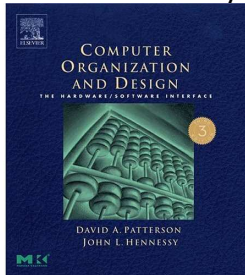
**Office Hours:** MW 10:20 am - 12:30 pm, F 11:30 am - 12:30 pm or by appointment

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**Lectures:** MWF 8:00 am - 9:00 am, HS 208

**Required Text: Computer Organization and Design, The Hardware/Software Interface**  
by John L. Hennessy, David A. Patterson, Morgan Kaufman Publishers, Inc.



**Web site for the course:** [http://www.uwosh.edu/faculty\\_staff/georgiev/subjects/CSC310/](http://www.uwosh.edu/faculty_staff/georgiev/subjects/CSC310/)

### Course Objective:

An introduction to computer hardware organization and architecture. Emphasis is given to the design of Central Processing Units, Arithmetic and Logic Units, and main memories. A comparison of alternate computer organizations is presented.

This course concentrates on the relationship between computing hardware and machine language instruction sets. The study is organized into levels, beginning with logic gates, through microcode, machine language and assembly language.

### Course Learning Outcomes:

#### Outcomes #1

- a) describe the various ways that computer performance can be measured and explain the pros and cons of each
- b) explain the issues associated with instruction set architecture design
- c) use the CPU performance equation to compare the performance of processor architectures
- d) apply Amdahl's speedup law to understand the value of an architectural modification

#### Outcomes #2

- a) understand and describe the tradeoffs between complex instruction set computers (CISC) and reduced instruction set computers (RISC).
- b) understand how the fundamental mathematical operations such as addition, subtraction, multiplication, and division can be optimized with appropriate number representation, rounding, and digital circuit implementation schemes.

#### Outcomes #3

- a) understand the key principles used in creating datapath and designing the control for Singlecycle and Multicycle architecture.

- b) see how the choice of various implementation strategies affects the clock rate & CPI for the machine.
- c) distinguish between Microprogrammed and Hardwired processor control, and describe the benefits of each approach.
- d) explain the concept of and describe the challenges associated with instruction level parallelism
- e) describe the general design of a processor that implements instruction level parallelism
- f) describe how dynamic scheduling overcomes data hazards
- g) describe how dynamic hardware prediction can reduce branch penalties
- h) discuss the various techniques to implement branch prediction
- i) give examples of how a compiler can exploit instruction level parallelism
- j) analyze the performance of a code segment in a given instruction execution pipeline
- k) identify data, control and structural hazards for a given processor architecture/code segment pair

#### Outcomes #4

- a) describe how a cache works and the various cache configurations
- b) enumerate various methods for enhancing cache and memory performance
- c) distinguish between Directly-Mapped Cache, Associative Cache, and Set-Associative Cache, and describe the principal issues related to cache memory organization;
- d) describe the importance of the hit ratio to the effectiveness of the cache memory;

#### Outcomes #5

- a) demonstrate ability to work effectively in teams.
- b) demonstrate the ability for effective verbal and written communication, performing an in-depth investigation of computer architecture related topic and present their findings to their classmates in an oral and written report.

#### **Course Requirements:**

There will be three exams, unannounced quizzes, assignments, and one presentation. The material for all exams will come from either a material covered in class, homework problems, and/or assignment reading.

Complete all required work on time. In the event that an exam must be missed, or required work can not be completed on time, due to illness or other serious and unavoidable circumstance, notify the professor as far in advance as possible by phone or e-mail.

You are encouraged to work in groups on your assignments. You can discuss assigned problems with other people or groups, but you must individually design and write your own (group) solutions/code for assignments. Submitting modified versions of other people's or group's work as your own is considered cheating.

If you work in a team, you will submit one electronic copy and one paper copy of the assignment with names on it and percent of participation (e.g. equal). Partners will earn equal

scores on the assignment. You may work alone on some assignments and in a team on others. You may change the team during the semester.

The assignments are due by 9:00 on the due date (electronic copy e-mail is due by 9:00 am, and a paper (hard) copy of the assignment is due at the beginning of class). Assignments will be accepted up to three days late subject to the following penalties:

Turned in	Penalty
After 9:00 am on the due date	10%
1 day late	25%
2 days late	50%
3 days late	75%

Saturdays, Sundays, and holidays count when computing penalties.

There will be no make up for unannounced quizzes.

There will be one make up for the exams, which will cover all topics. It will be at the end of the semester.

Make up will be given if you call before the exam, make arrangements, have a medical certificate signed by the physician, and have a note from the Dean of Students Office.

The three exams will be announced at least a week before taking place.

### **Evaluation:**

Three Exams (equal weight): ~60%

Unannounced quizzes and class work (equal weight): ~10%

Assignments (equal weight): ~25%

Presentation: ~5%

### **Course Outline:**

- ◆ Instruction Set Design: Cost and Performance.
- ◆ Computer System Design: Single- & Multi-Cycle.
- ◆ Data Path Design: ALU, Multipliers, Registers, ....
- ◆ Instruction Sequencing and Control: FSM & Microcode.
- ◆ Pipeline Design: Fundamental Principles.
- ◆ Memory Systems: RAM, Cache, Memory Hierarchies.
- ◆ Input – Output and Communications: busses.

Your grade will be based on the following scale:

<b>Score</b>	<b>Grade</b>
$\geq 92$	A
90-92	AB
82-90	B
80-82	BC
72-80	C
70-72	CD
60-69	D
$< 60$	F

**Feedback:**

Your comments and questions about all aspects of the course (content, grading, teaching methods, pace, textbook, etc) are welcome. You can use e-mail or talk to me during office hours.